ABSTRACT OF THE DISCLOSURE

A circuit architecture and a method perform a page programming in non-volatile memory electronic devices equipped with a memory cell matrix and an SPI serial communication interface, as well as circuit portions associated to the cell matrix and responsible for the addressing, decoding, reading, writing and erasing of the memory cell content. Advantageously, a buffer memory bank is provided to store and output data during the page programming in the pseudo-serial mode through the interface. Data latching is performed one bit at a time and the following outputting occurs instead with at least two bytes at a time.